In the Claims:

Add new claims 10 and 11 as follows:

10. The semiconductor device as claimed in claim 9, further comprising a static random access memory section having memory cells, a logic circuit section, and an interface section, wherein the interface section includes said first and second MOS transistors.

11. The semiconductor device as claimed in claim 9, wherein said first MOS transistors operate at a first voltage and said second MOS transistors operate at a second voltage higher than the first voltage.